Atty. Docket No. OPP031034US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Dae-Gun LEE : GROUP ART UNIT: 2826

APPLICATION NO: 10/734,818 :

FILED: December 12, 2003 : EXAMINER: Pert, Evan T.

FOR: METHODS TO FABRICATE A SEMICONDUCTOR DEVICE

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 13, 2005.

By: ______________________
Amanda Tost

DECLARATION UNDER 37 C.F.R. 1.132

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SIR:

I, Jong-chul LIM, hereby declare and state that:

1. I am currently employed by Dongbu Electronics Co., Ltd. (hereinafter, "DBE") as an Assistant Manager in the Technology Alliance Team. My responsibilities include managing, overseeing and coordinating activities relating to the patent portfolio of DBE, including certain Korean, U.S. and other international patent applications of DBE.

2. I have been continuously employed by DBE since November 1, 2003. I received a Master's degree in Chemical Engineering, with emphasis in Semiconductor Process technology,

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from San Jose State University in 2004. As one having skill in the art of fabrication of semiconductor devices, I am familiar with the subject matter disclosed and claimed in the above-identified application.

3. I have read and reviewed the above-identified application, the Amendment filed on February 21, 2006, the Office Action dated May 12, 2006, and U.S. Patent No. 4,376,672 to Wang et al. (hereinafter, "Wang").

4. I understand that the broadest claims of the above-identified application are directed to a method to fabricate a semiconductor device. In one aspect, the method includes:

forming a nitride layer on an interlayer insulating layer;

forming a photoresist layer on the nitride layer;

forming a photoresist pattern from the photoresist layer, the photoresist pattern having a thickness that depends on a thickness and an etch rate of the interlayer insulating layer and an etch rate of the photoresist pattern;

etching the nitride layer using the photoresist pattern as a mask;

etching the interlayer insulating layer together with the photoresist pattern; and

setting an etch stop point as a point at which the photoresist pattern is removed by etching.

5. In another aspect, the method includes:

forming a first mask layer on an etch target layer;

forming a second mask layer on the first mask layer;

forming a first mask pattern by selectively etching the second mask layer, the first mask pattern having a thickness that depends on a thickness and an etch rate of the etch target layer and an etch rate of first mask pattern;

forming a second mask pattern by etching the first mask layer using the first mask pattern as a mask;

etching the etch target layer together with the first mask pattern, wherein the first mask pattern is etched using the second mask pattern as a mask; and

setting an etch stop point at which the first mask pattern is removed by etching (see, e.g., Claim 1 as originally filed).

6. In further aspects, the method includes setting an etch stop point as a point at which the nitride layer or the second mask pattern is exposed.

7. The subject matter described in paragraphs 4-6 above is described in the original specification in such a way as to reasonably convey to one skilled in the art that I had possession of that subject matter at the time the application the was filed. In addition, a person skilled in the art is capable of using the present invention based on the original specification without undue experimentation.

8. The Examiner appears to understand at least part of the inventive concept as recited in paragraphs 4-6 above (see, e.g., the first full paragraph on page 5 of the Office Action dated May 12, 2006). At least part of the inventive concept involves recognizing that a second mask pattern (e.g., a nitride layer as recited in paragraphs 4-5 above, or a "hard mask" as identified by the Examiner on page 5 of the Office Action) can be used to set an etch stop point for (simultaneously) etching a first mask pattern (e.g., a photoresist pattern as recited in paragraphs 4-5 above, or a "photoresist" as identified by the Examiner on page 5 of the Office Action) on the second mask pattern and an etch target layer (e.g., an interlayer insulating layer as recited in paragraphs 4-5 above, or "an insulating layer" as identified by the Examiner on page 5 of the Office Action), by use of a point at which either the first mask pattern is removed by etching (e.g., paragraphs 4 and 6 above) or the second mask pattern is exposed (e.g., paragraphs 5-6 above).

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9. One skilled in the art of semiconductor manufacturing (and, in particular, etching material layers in semiconductor devices using masks) would readily understand from the application as originally filed how to make and use the invention, without reference to specific materials, etchants or etch processes, which generally depend on the recipe for a particular fabrication process.

10. The application as originally filed discloses that the photoresist pattern is etched together with the interlayer insulating layer during an interlayer insulating layer etching process (see, e.g., paragraph [0013], page 3; and paragraph [0013], page 4). This disclosure is reflected in the language of paragraph 4 above (e.g., "'etching the interlayer insulating layer together with the photoresist pattern…"; "etching the etch target layer together with the first mask pattern…," as recited in paragraph 5 above).

11. As is further disclosed in paragraph [0015] of the application as originally filed, the etching process is terminated by setting the time point when the photoresist pattern is entirely removed such that the nitride layer is exposed by the etching process. Also, as is further disclosed in paragraph [0013] of the application as originally filed (pages 3-4), the thickness of the photoresist pattern is determined by considering the thickness and etch rate of the interlayer insulating layer and the etch rate of the photoresist pattern.

12. One skilled in the art thus understands from paragraphs [0013] and [0015] of the application as originally filed that, from just the thicknesses and the etch rates of the interlayer insulating layer and the photoresist pattern, one can set an etch stop point for etching the photoresist pattern (the first mask pattern) and the interlayer insulating layer (the etch target layer) as the point at which (i) the photoresist pattern is removed by etching or (ii) the nitride layer is exposed.

13. It is within the abilities of those skilled in the art to determine a desired thickness for nearly any material used conventionally in semiconductor manufacturing from a deposition rate or growth rate and a length of the deposition (or growth) time. To obtain a sufficiently accurate rate, one skilled in the art generally determines a deposition rate or growth rate for a

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given material empirically, on a given apparatus (or equipment) and under a given set of operational conditions (usually starting with a default set of conditions for the given material and the given apparatus or equipment). Thus, it does not require undue experimentation to determine a thickness for nearly any given material used conventionally in semiconductor manufacturing.

14. Similarly, it is within the abilities of those skilled in the art to determine an etch rate for nearly any material used conventionally in semiconductor manufacturing using a particular apparatus (or equipment), a known etchant chemistry for a particular material, and a given set of operational conditions. To obtain a sufficiently accurate etch rate, one skilled in the art generally determines the etch rate for a particular material empirically, on a given apparatus (or equipment), using a given etchant chemistry (usually a default or recommended etchant chemistry for the particular material), under a given set of operational conditions (usually starting with a default set of conditions for the given apparatus or equipment, the given etchant chemistry, and the particular material). Thus, it does not require undue experimentation to determine an etch rate for nearly any material used conventionally in semiconductor manufacturing.

15. It is known in the art that an end point of a process for etching a transparent or non-transparent material can be monitored using laser interferometry or laser reflectance, respectively (see, e.g., Wolf, S., *Silicon Processing for the VLSI Era*, vol. 1 (2000), Lattice Press, Sunset Beach, California; particularly the first paragraph of § 14.7.1, pp. 695-696, attached hereto ("Wolf")). It is further known in the art that both photoresists and a nitride layer (e.g., silicon nitride) can be used to monitor an end point of an etching process using optical emission spectroscopy (Wolf, p. 697, attached hereto). Although these end point monitoring techniques may have limitations or other drawbacks, the limitations and/or drawbacks are known, and do not render the present invention inoperable.

16. The application as originally filed includes a number of examples of how to make and use the invention. For example, paragraph [0016] on page 4 of the application as originally filed states that when the respective etch rates of the interlayer insulating layer and the

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photoresist pattern are about 5000 Å/min and about 1800 Å/min, the interlayer insulating layer is formed to have a thickness of about 7500 Å, and the photoresist pattern (after etching the nitride layer) has a thickness of about 2500 Å. As a result, the photoresist pattern is entirely removed when about 7000 Å of the interlayer insulating layer is etched, thereby exposing the nitride layer.

17. Therefore, as described in the present application, when the second (photoresist) mask layer is thick enough, it can be used as an etching mask (e.g., to etch the first mask (nitride) layer, see paragraph [0014] of the original description), and when etching time is long enough, the photoresist layer can be completely etched along with the target (insulating) layer (e.g., by exposing the first mask (nitride) layer to determine the etch end point; see, e.g., paragraph [0015] of the original description).

18. Therefore, it is well within the abilities of a person skilled in the art to select specific mask materials (e.g., photoresists and nitrides), specific etch target (e.g., interlayer insulator) materials, and specific etchant(s) and/or etch processes (as well as to select specific thicknesses of each of the materials consistent with the easily determined deposition/growth rates thereof) in order to carry out the steps — and obtain the results — of the present invention.

19. Accordingly, the subject matter of paragraphs 4-6 are fully enabled by the application as filed.

20. Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

Atty. Docket No. OFP03101/4US
Serial No: 10/734,818

Jong-chul LIM

Aug. 8, 2006
Date

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1: PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.
RICHARD N. TAUBER Ph.D.

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dried in high-temperature-nitrogen after such a water rinse. Additional practices which have proven effective involve exposing the etched and stripped wafers to a fluorine containing plasma. The highly reactive fluorine radicals readily displace chlorine that is bound to the aluminum. These Al-F bonds are very stable, and do not react with water. Another technique is to regrow the protective native oxide on the Al surface. This may be done in a furnace at 300–400°C in an oxygen ambient for 30–60 minutes. This not only grows the oxide but also tends to drive off any remaining chlorine. Thus, there are numerous ways to attack the problem of Al corrosion after dry etch. Generally speaking, more than one of them must be employed to yield an Al etch process in which corrosion is under control. The particular techniques chosen depend on the alloy being etched and the tools available to do the etching.

14.6.6 Etching Organic Films

Organic films are exposed to plasma etching environments in many applications during ULSI fabrication. Photoresist is most commonly used as an etch mask, and in such applications it is usually desired that the resist not be etched by the plasma. In some cases, however, the resist is deliberately etched as part of a technique used to produce directional etching effects in underlying films (e.g., sloped contact sidewalls), or as a method for producing planarization of layers under the resist. In some instances the etch rate of the resist must be accurately known and controlled. At the conclusion of the pattern etching step the resist must be removed, and this can be achieved by a plasma etch process as well. Organic film etching is also performed in dry-developable resist and tri-layer resist processes (Chap. 12), and in etching polyimide films.

Plasmas containing pure oxygen at moderate pressures produce species that attack organic materials to form CO, CO_2, and H_2O as end products.[2,57] Such oxygen plasmas provide a highly selective method for removing organic materials, since the O_2 plasmas do not etch Si, SiO_2, or Al. The addition of fluorine-containing gases to the O_2 causes the etch rate of organic materials to significantly increase. This occurs because the F atoms extract hydrogen from the organic films to form HF, producing sites that react more rapidly with molecular oxygen.

14.7 PROCESS MONITORING AND ENDPOINT DETECTION

Dry etch equipment used in a ULSI production environment requires the availability of effective diagnostic and etch endpoint detection tools. Extremely tight control of all process parameters must be maintained to ensure wafer-to-wafer reproducibility. In typical production facilities, some of these parameters can be controlled, while others cannot. For example, reactor wall conditions (which contribute to the heterogeneous destruction of active reactants), become a *bona fide* variable if the walls are exposed to atmosphere after every run. (This is one reason why single-wafer reaction chambers are not exposed to the ambient between wafers.) Similarly, outgassing, virtual leaks, and backstreaming from pumps can sufficiently change the chemistry, so that a calibrated etch-time approach to reproducibility generally proves to be inadequate. Thus, techniques for determining the endpoint of a cycle become highly valuable as procedures which can reduce the degree for overetching, and for increasing throughput and reproducibility. In this section two common methods for determining the endpoint of dry etch processes are described: 1) laser interferometry and reflectivity, and 2) optical emission spectroscopy.

14.7.1 Laser Interferometry and Laser Reflectance

Laser interferometry monitors the thickness of *optically transparent* films on reflective substrates by making use of interference effects. The *laser reflectance method* exploits the differ-

ence in the reflectivity between a *non-transparent* material being etched and an underlying layer. The same apparatus can be utilized to carry out both techniques, and is shown in Fig. 14-34b. The system is designed to measure the intensity of light reflected from films being monitored.

In the case where a transparent film is being etched (e.g., SiO_2), the amplitude of the intensity of the reflected light varies in approximately a sinusoidal manner as interference conditions change with decreasing film thickness. If the incident light is normal to the surface, the film thickness change Δd between any two adjacent maxima or minima is given by $\Delta d = \lambda/2n$, where λ is the wavelength of the incident light, and n is the index of refraction of the etched layer. If the etch time between two adjacent maxima is known, *in situ* etch rates can be inferred. Laser interferometry can also provide endpoint detection. That is, the interface between two dielectrics is identifiable as a change in slope caused by the different refractive indices, and by a change in the frequency of the reflectance variations due to the etch rate variations of the two materials.

Opaque/transparent interfaces (e.g., metal/dielectric) are distinguished by a variation from an approximately constant reflectivity to an oscillating one. In the case when *two nontransparent films* are etched there is a change in the reflected signal when the endpoint is reached (if the reflectivity of the underlying layer differs significantly from the film being etched). This change is proportional to the ratio of the reflectivity of the layer being etched to the underlying layer. Of course, the *laser reflectance* method does not provide any information on the *in situ* etch rate, and therefore does not provide as much information as *laser interferometry*.

These techniques have several limitations. First, the laser must be focused on a flat region of the wafer on which the film being etched is exposed. Thus, in many etching applications, where the area being etched is too small for good reflectivity measurements (e.g., etching of contacts in an SiO_2 film), a larger test site (> 0.5 mm) must be added to the wafer patterning to facilitate this measurement. This requirement can be costly, as the open space must be located in a prime area of the wafer. Even when such a test area is present, each wafer must be accurately aligned, so that the laser light is incident on this area during the etch process. Second, this method provides etching information only on a limited area of the wafer surface. Finally, the output signal is weak if the etched surface is rough.

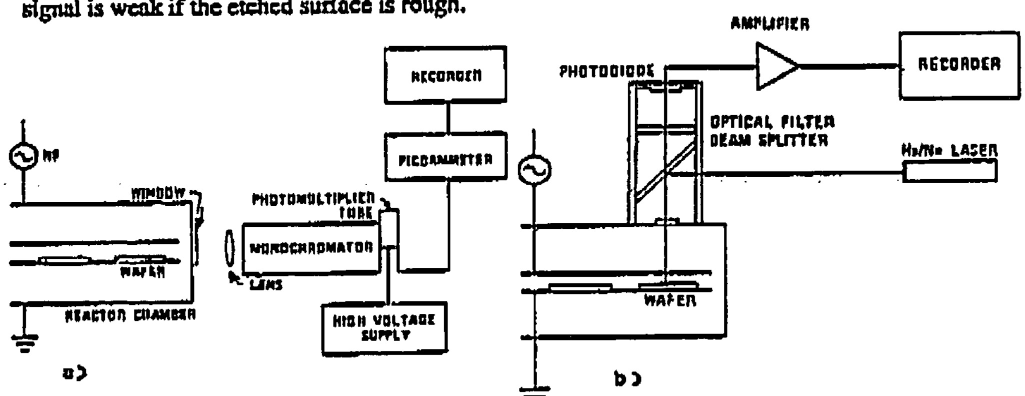

Fig. 14-34 (a) Experimental apparatus for using emission spectroscopy as an end point detector; (b) Typical apparatus for the optical reflection method of end point detection.[58] Reprinted by permission of Solid State Technology, published by PennWell.

14.7.2 Optical Emission Spectroscopy

Optical emission spectroscopy is the most widely used method for endpoint detection because it is easy to implement. It can offer high sensitivity and it provides useful information about both etching species and etch products. The technique relies on the change in the emission intensity of characteristic optical radiation, from either a reactant or product in a plasma. Light is emitted by excited atoms or molecules when electrons relax from a higher energy state to a lower one. Atoms and molecules emit a series of spectral lines that is unique to each species. The emission intensity is a function of the relative concentration of a species in the plasma. A typical apparatus utilized for endpoint detection is shown in Fig. 14-34a. It operates by recording the emission spectrum during the etch process in the presence and absence of the material that is to be etched. A detector is equipped with a filter that lets light of specific wavelengths pass through to be detected. To detect the end point, the emission intensity of the process-sensitive line (or band) is monitored at a fixed wavelength. When the end point is reached, the emission intensity changes. The change in emission intensity at the endpoint depends on the species being monitored. The intensity due to reactive species increases, while the intensity due to etch products decreases.

It is useful to monitor emission from both reactive species and product species simultaneously (Table 14-3), because in some etching applications one or the other of these measurements may yield a stronger signal.[3] Optical emission spectroscopy is widely used for determining the endpoint of SiO_2, polysilicon, and aluminum layers. In batch etch processes the endpoint signal is derived from the average of etch conditions in the process. As a result, some timed overetching is still required to insure that all wafers have been completely etched.

Optical emission spectroscopy also has some drawbacks. One of the most important is that its sensitivity is determined by the etch rate and the total area being etched. Thus, for slow etch processes the endpoint may be difficult to detect. The fact that the sensitivity is also dependent on the total area being etched, in some instances requires a special test site be established to provide sufficient exposed area to cause a detectable end point signal (e.g., ~1 cm^2 of exposed Si[58]). Separate test sites are needed most when small contacts are being etched (i.e., the total area of etched surface is small), or when the etch depths become comparable to the separation

Table 14-3 SPECIES AND EMISSION WAVELENGTH FOR OPTICAL EMISSION ENDPOINT DETECTION[58]

FILM	SPECIES MONITORED	WAVELENGTH (nm)
Resist	CO	297.7, 483.5, 519.8
	OH	308.9
	H	656.3
Silicon, Polysilicon	F	704
	SiF	777
Silicon Nitride	F	704
	CN	387
	N	674
Aluminum	AlCl	261.4
	Al	396

between features. In the latter case, the total area (sidewall + bottom) of material being etched can remain almost constant, even after the bottom of the film has been reached and only undercutting is occurring.

14.8 DRY-ETCH EQUIPMENT CONFIGURATIONS

Plasma etching systems consist of several components: a) an etching chamber (that is evacuated to reduced pressures); b) a pumping system for establishing and maintaining the reduced pressure; c) pressure gauges to monitor pressure in the chamber; d) a variable conductance between the pump and etching chamber so that the pressure and flow rate in the chamber can be controlled independently; e) one (or two) rf power supplies to create the glow discharge; f) a gas handling capability to meter and control the flow of reactant gases; g) electrodes; and h) in etch tools for sub-micron applications, a vacuum load-lock that isolates the chamber from the ambient and a robot that transfers wafers from the cassettes through the load-lock and into the etch chamber. Detailed assembly of such systems from these components has evolved a variety of configurations, depending upon which parameters of a process need to be controlled, as well as the specific applications of the system.[59]

Several of the most important commercially available plasma etch/RIE etch system configurations will now be described. Some of this discussion is historical, insofar as it covers the batch etching tools used for wafers up to 150-mm in size. These include: 1) barrel etchers; 2) parallel-electrode (planar) reactor etchers; and 3) hexode batch etchers. Then single-wafer etchers are discussed, including: 1) conventional parallel-plate etchers; 2) downstream etchers; and 3) magnetically-enhanced reactive ion etchers. Finally, etch tools based on high-density plasma sources (which are the newest types of dry-etching tools) are covered.

14.8.1 Batch Commercial Dry-Etch System Configurations

14.8.1.1 Barrel Etchers: The first, and simplest, plasma etchers to be developed[60] were barrel etchers (Fig. 14-35a). This configuration consists of a cylindrical reaction vessel, usually made of quartz, with rf power supplied by metal electrodes placed above and below the cylinder. A perforated metal cylindrical *etch tunnel* is placed within the etch chamber. This serves to confine the glow discharge to the annular region between the etch tunnel and the chamber wall. Wafers are placed in a holder or *boat* at the center of the cylinder, and usually no electrical connection is made to them. The reactive species created by the discharge diffuse to the region within the etch tunnel, but the energetic ions and electrons of the plasma do not enter this region. The reactive species of the plasma diffuse to the surfaces to be etched. Since there is no ionic bombardment, the etching is almost purely chemical. As a result, etching tends to be isotropic, and it is possible to obtain good selectivity with little or no radiation damage. Most barrel etchers are operated in the high-pressure range of dry etching (0.5–2.0 torr). The isotropic nature of the etch, however, now limits barrel etchers to such applications as resist stripping in ICs with feature sizes > 1 μm.

14.8.1.2 Parallel Electrode (Planar) Reactors: As described earlier, wafers exposed to energetic ions of a plasma can be subjected to ion-assisted etching processes. Etcher configurations that utilize parallel electrodes can direct energetic ions at the surfaces being etched, by causing them to be accelerated across the potential difference that exists between the plasma and the electrode surfaces (Fig. 14-11b). As a result, both a physical and a chemical component can impart directionality to the etch process.